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**\*BIBDATASHEET\***

CONFIRMATION NO. 4078

Bib Data Sheet

SERIAL NUMBER 10/736,356	FILING DATE 12/15/2003  RULE	CLASS 324	GROUP ART UNIT 2829	ATTORNEY DOCKET NO. P2000,0322 D
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**\*\* CONTINUING DATA \*\*\*\*\*** *E. J. K.*  
 This application is a DIV of 10/010,504 12/05/2001 PAT 6,762,611

**\*\* FOREIGN APPLICATIONS \*\*\*\*\*** *E. J. K.*  
 GERMANY 100 60 438.2 12/05/2000

IF REQUIRED, FOREIGN FILING LICENSE GRANTED  
**\*\* 03/24/2004**

Foreign Priority claimed <input checked="" type="checkbox"/> yes <input type="checkbox"/> no	STATE OR COUNTRY GERMANY	SHEETS DRAWING 4	TOTAL CLAIMS 6	INDEPENDENT CLAIMS 1
35 USC 119 (a-d) conditions met <input checked="" type="checkbox"/> yes <input type="checkbox"/> no <input type="checkbox"/> Met after Allowance				
Verified and Acknowledged <i>E. J. K.</i> Examiner's Signature Initials				

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TITLE  
 Method and probe card configuration for testing a plurality of integrated circuits in parallel

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